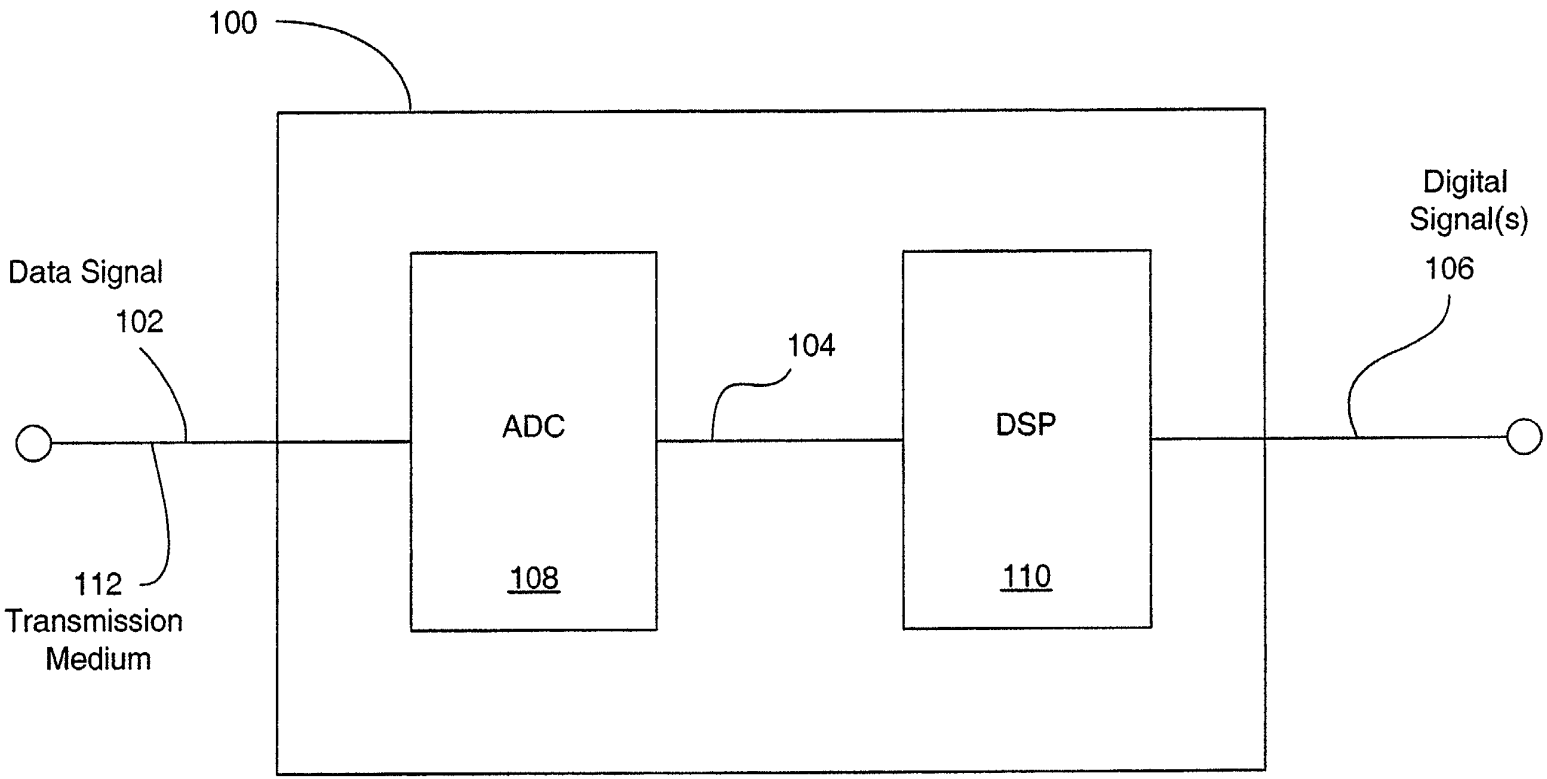

100
Data Signal
102
112
Transmission
Medium
ADC
108
104
DSP
110
Digital
Signal(s)
106

FIG. 1

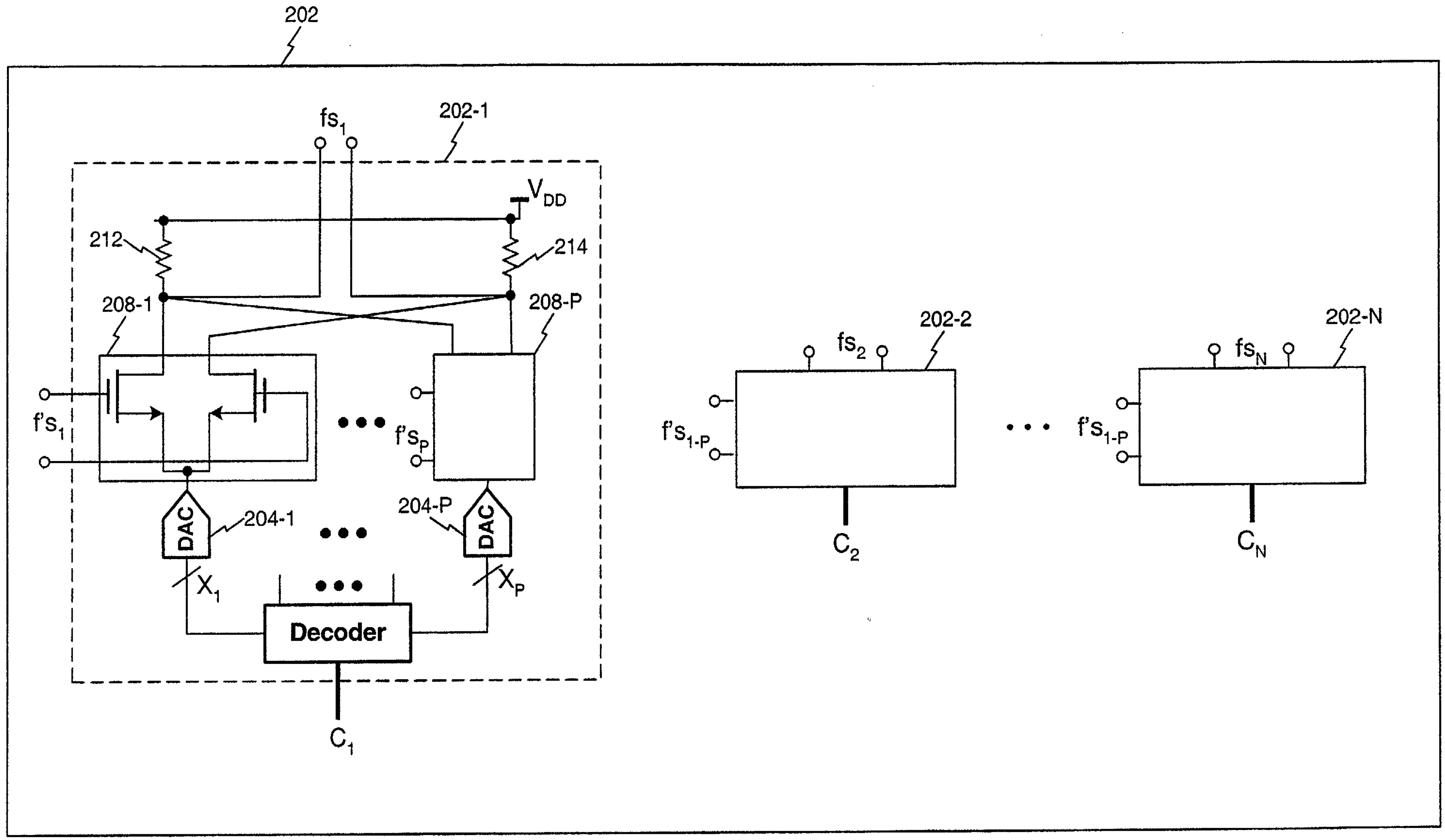

202
202-1
fs1
VDD
212
214
208-1
208-P
f's1
f'sP
204-1
204-P
DAC
DAC
X1
XP
Decoder
C1
202-2
fs2
f's1-P
C2
202-N
fsN
f's1-P
CN

FIG. 2

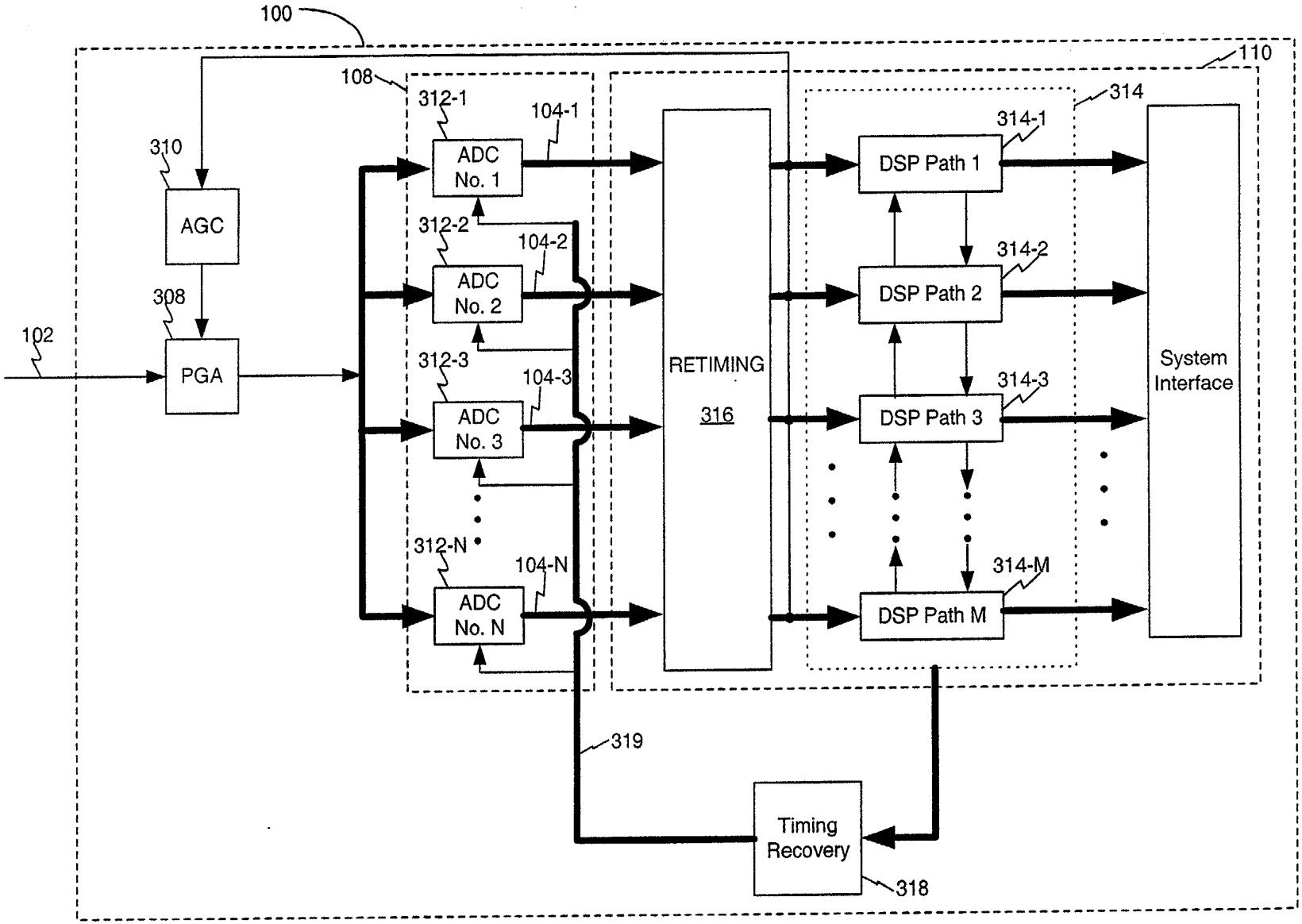

100
110
108
312-1
104-1
ADC No. 1
310
AGC
312-2
104-2
ADC No. 2
308
102
PGA
312-3
104-3
ADC No. 3
312-N
104-N
ADC No. N
RETIMING
316
314
314-1
DSP Path 1
314-2
DSP Path 2
314-3
DSP Path 3
314-M
DSP Path M
System Interface
319
Timing Recovery
318

FIG. 3A

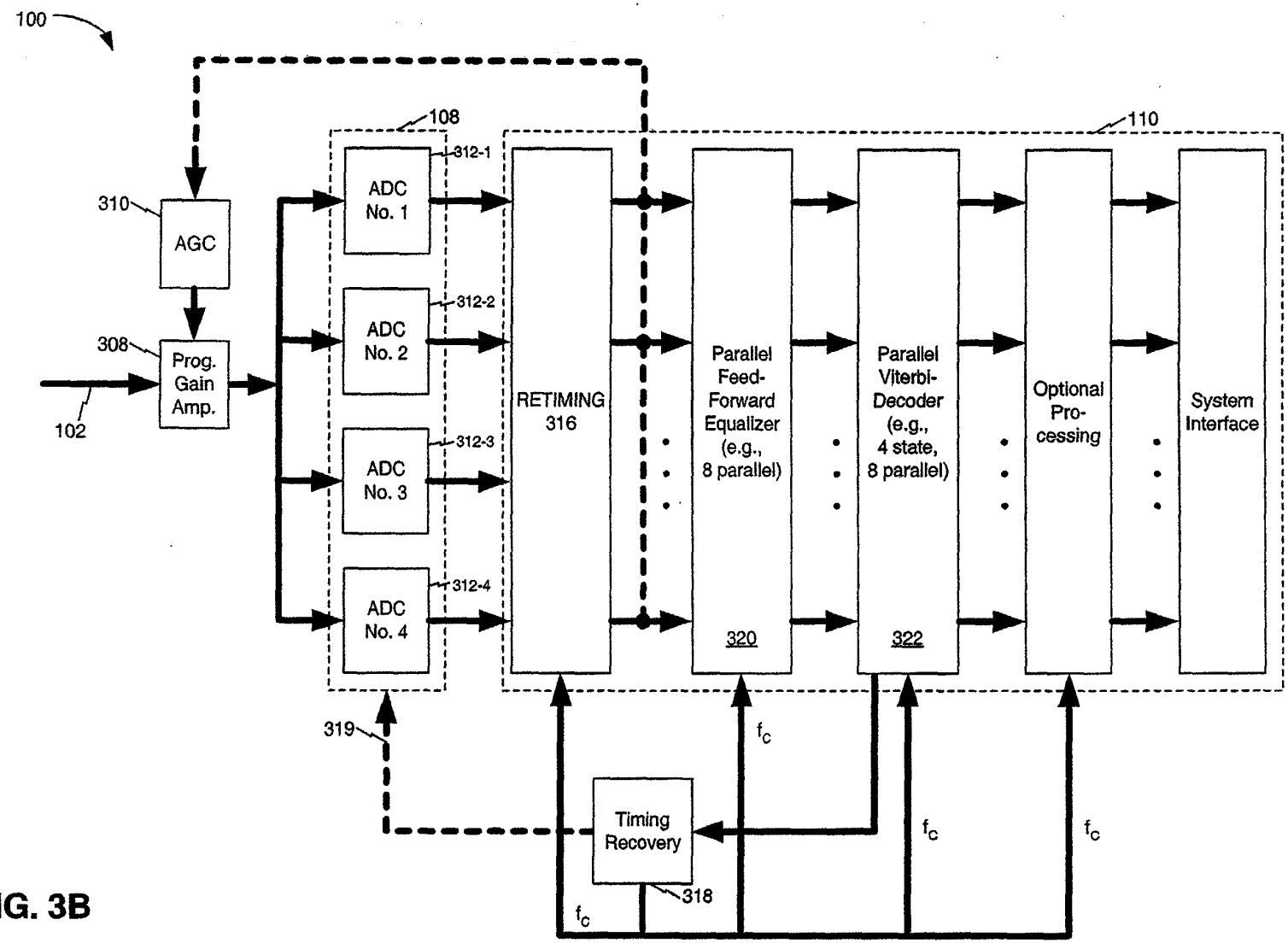

100
108
110
310
AGC
308
Prog. Gain Amp.
102
ADC No. 1
ADC No. 2
ADC No. 3
ADC No. 4
312-1
312-2
312-3
312-4
RETIMING 316
Parallel Feed-Forward Equalizer (e.g., 8 parallel)
320
Parallel Viterbi-Decoder (e.g., 4 state, 8 parallel)
322
Optional Pro-cessing
System Interface
319
Timing Recovery
318
f_c
f_c
f_c
f_c

FIG. 3B

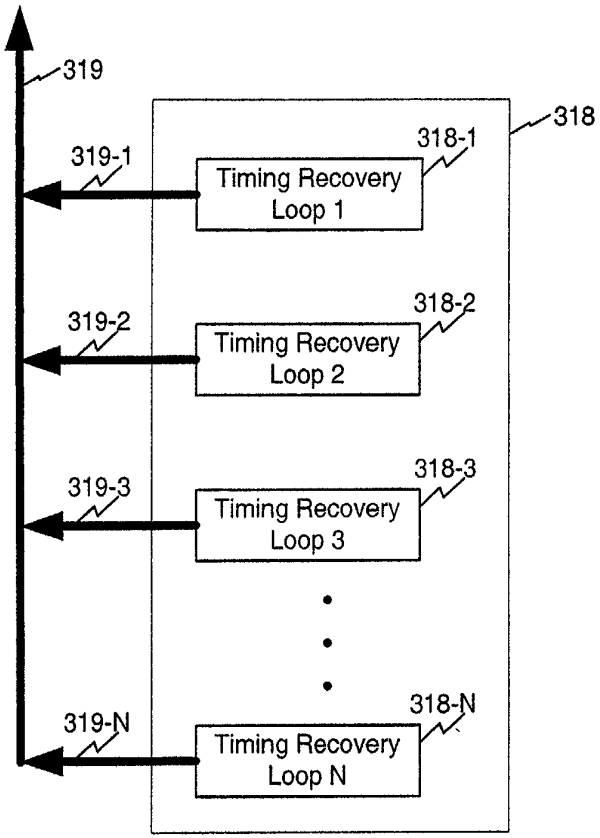

319
318
319-1
318-1
Timing Recovery Loop 1
319-2
318-2
Timing Recovery Loop 2
319-3
318-3
Timing Recovery Loop 3
319-N
318-N
Timing Recovery Loop N

FIG. 3C

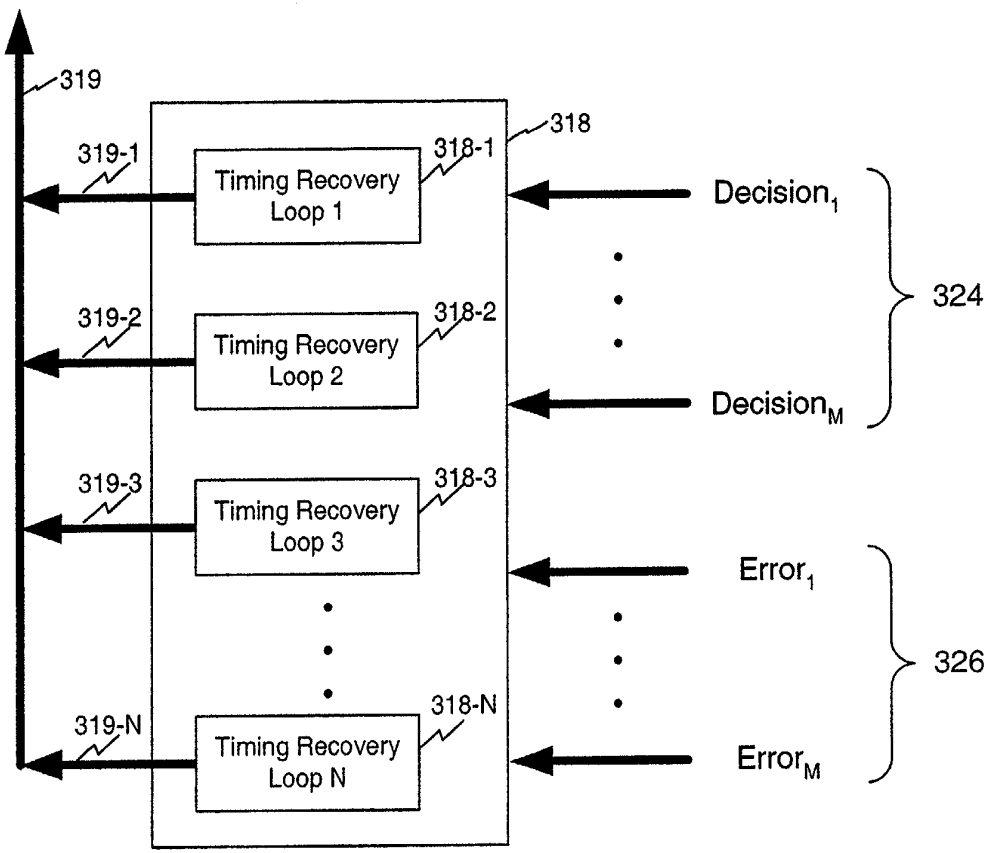

319
319-1
318-1
Timing Recovery Loop 1
318
Decision$_1$
319-2
318-2
Timing Recovery Loop 2
Decision$_M$
324
319-3
318-3
Timing Recovery Loop 3
Error$_1$
326
319-N
318-N
Timing Recovery Loop N
Error$_M$

FIG. 3D

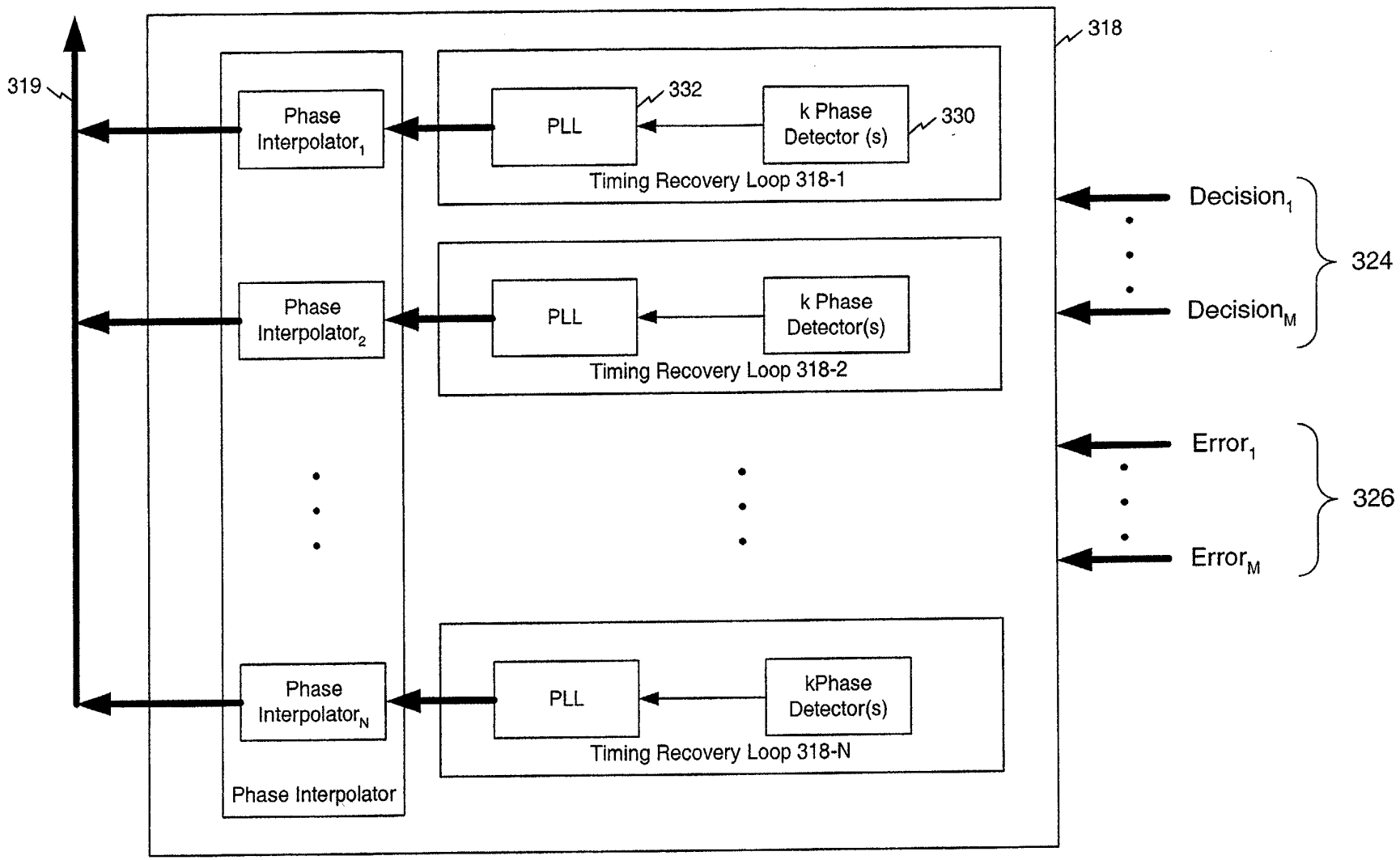

318
319
Phase Interpolator$_1$
PLL
332
k Phase Detector (s)
330
Timing Recovery Loop 318-1
Decision$_1$
Decision$_M$
324
Phase Interpolator$_2$
PLL
k Phase Detector(s)
Timing Recovery Loop 318-2
Error$_1$
Error$_M$
326
Phase Interpolator$_N$
PLL
kPhase Detector(s)
Timing Recovery Loop 318-N
Phase Interpolator

FIG. 3E

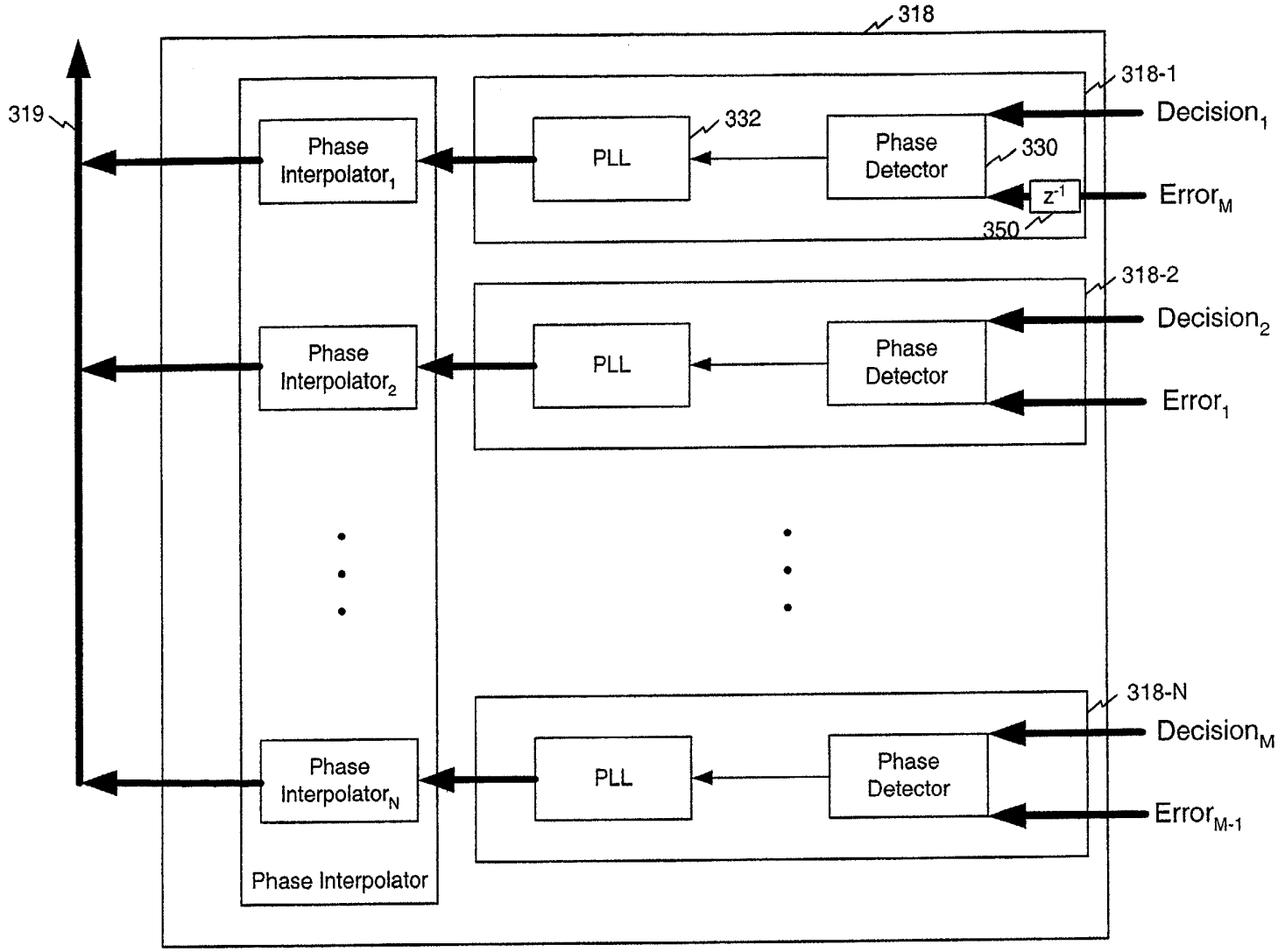


FIG. 3F

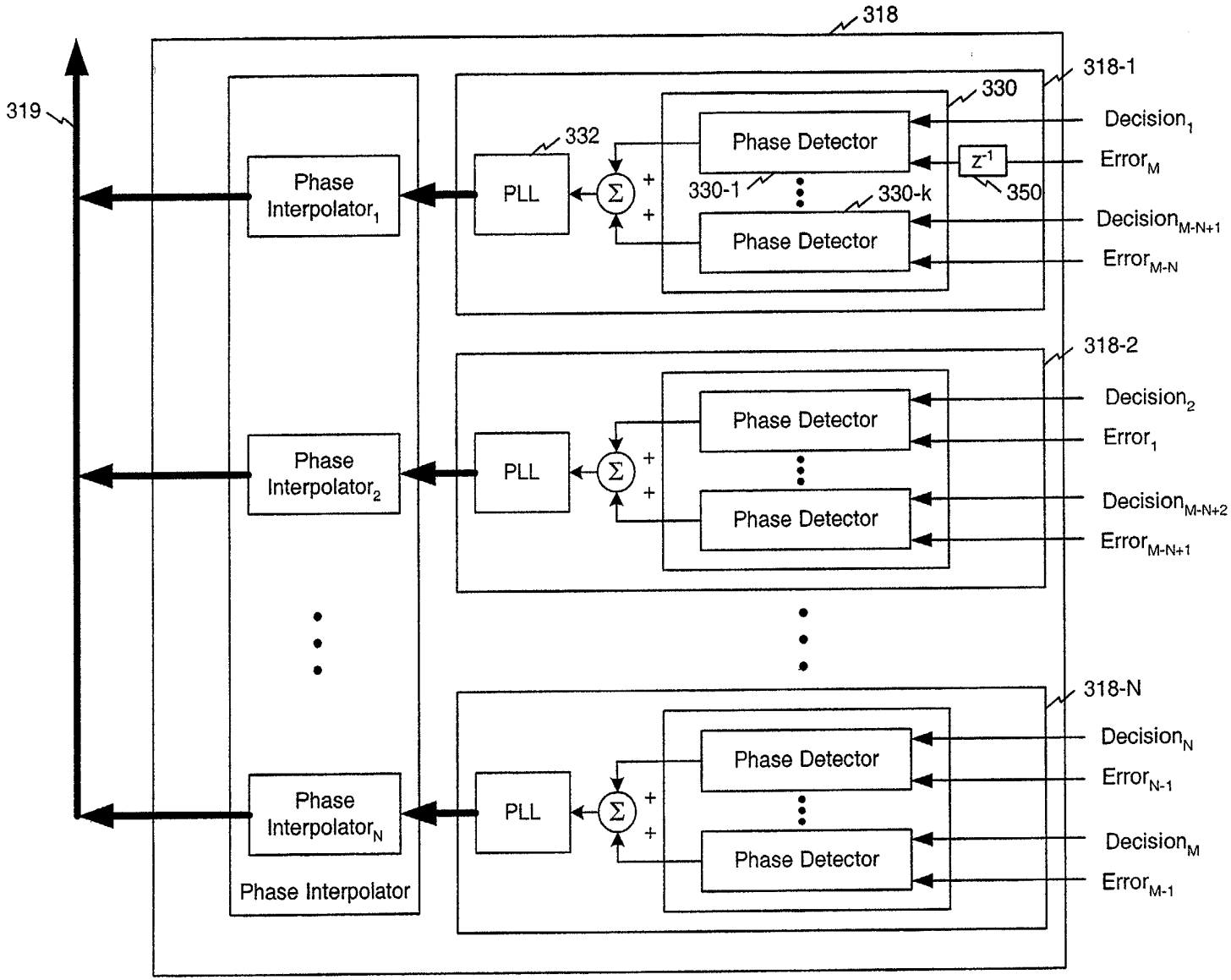

318
319
318-1
330
332
Phase Detector
PLL
Phase Interpolator1
330-1
330-k
Phase Detector
Z-1
350
Decision1
ErrorM
DecisionM-N+1
ErrorM-N
318-2
Decision2
Error1
DecisionM-N+2
ErrorM-N+1
318-N
DecisionN
ErrorN-1
DecisionM
ErrorM-1
Phase Interpolator2
PhaseInterpolatorN
Phase Interpolator
Σ
+
+

FIG. 3G

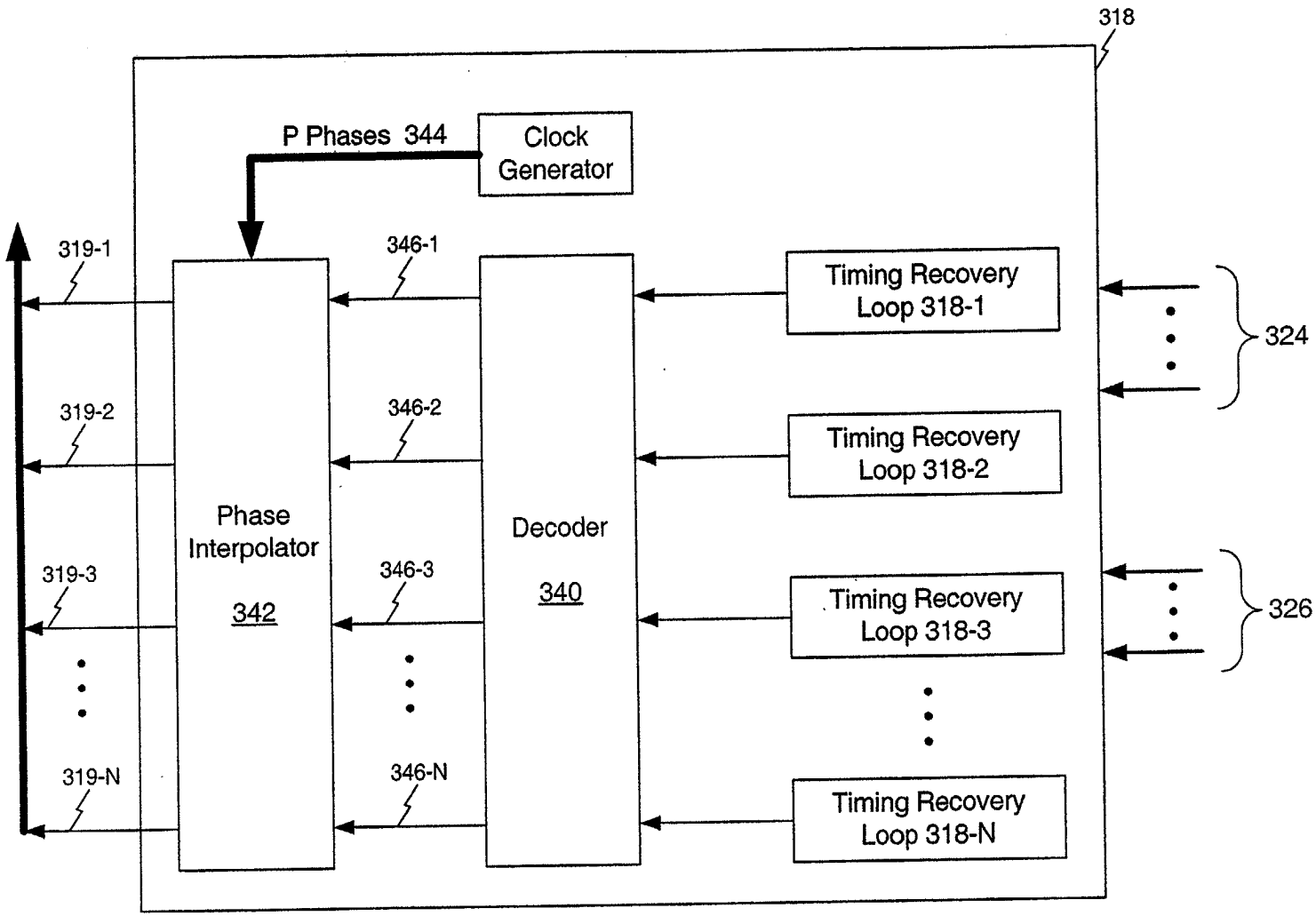


FIG. 3H

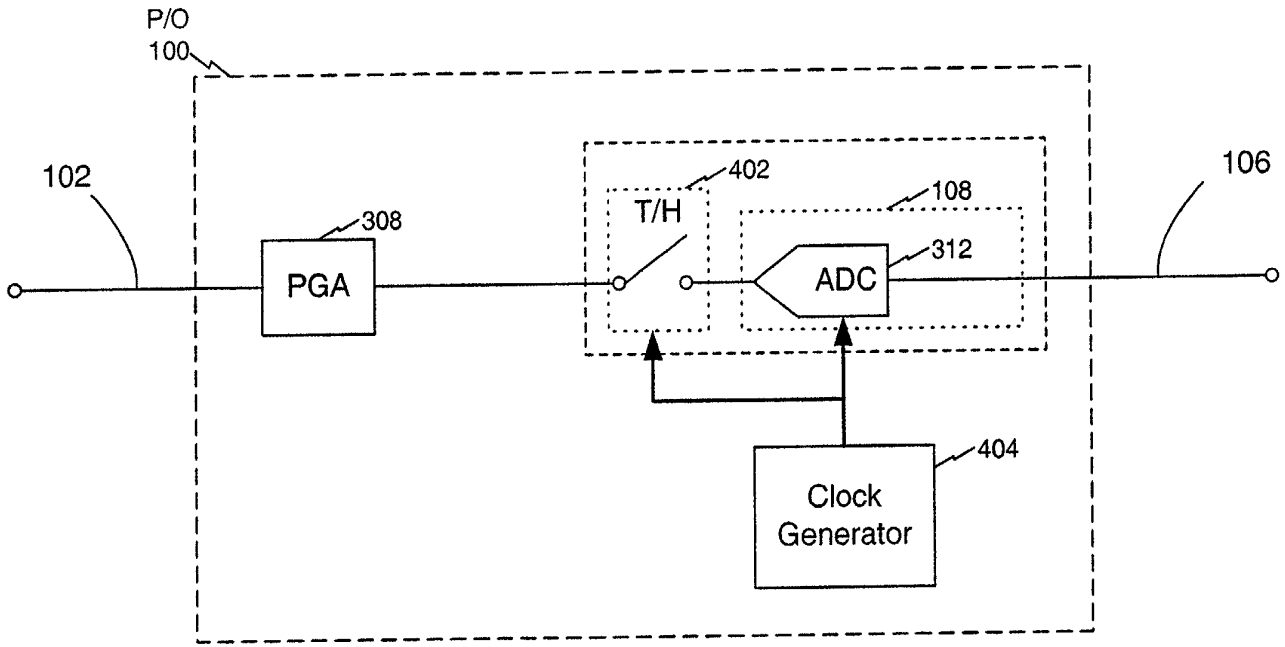


FIG. 4A

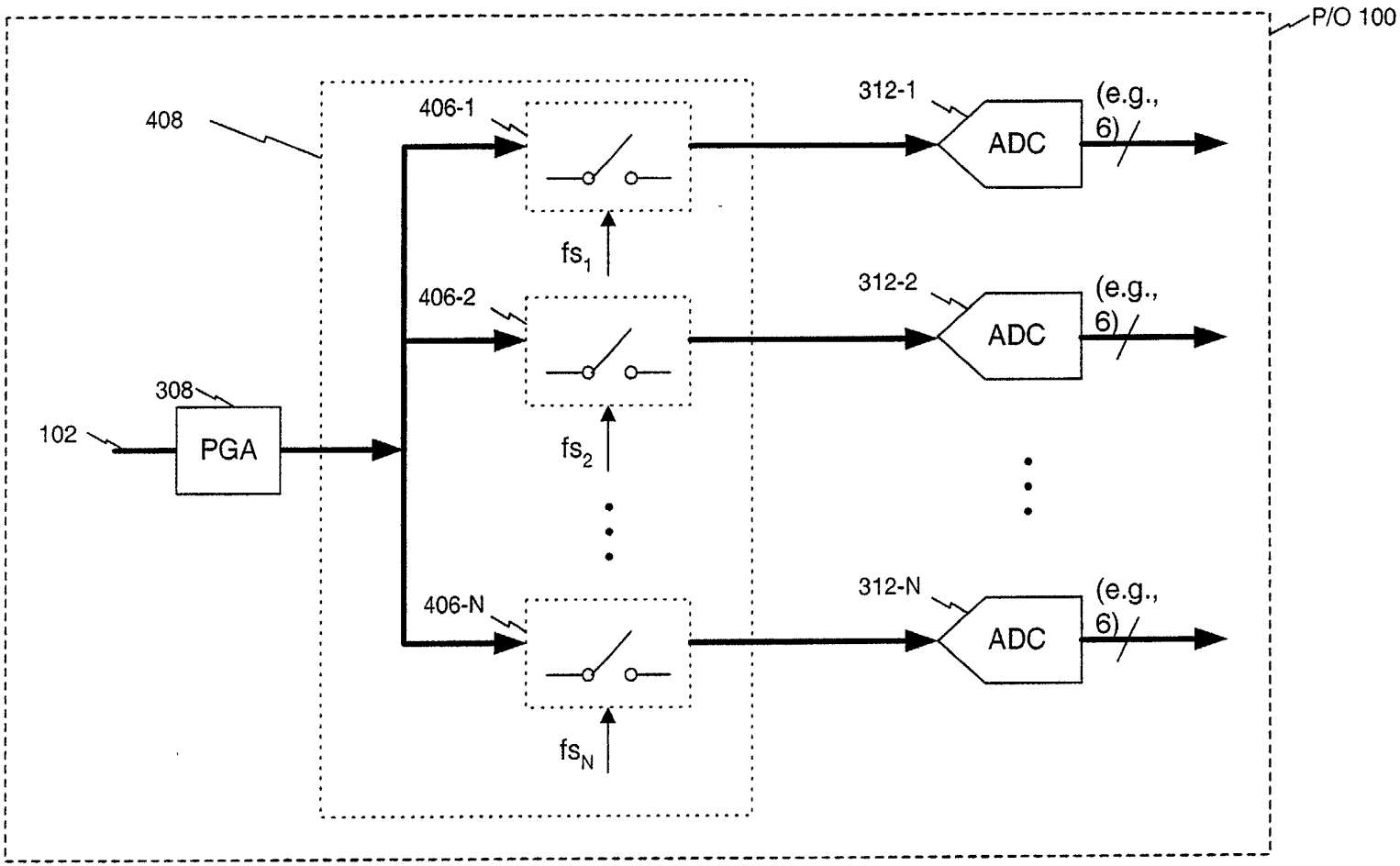


FIG. 4B

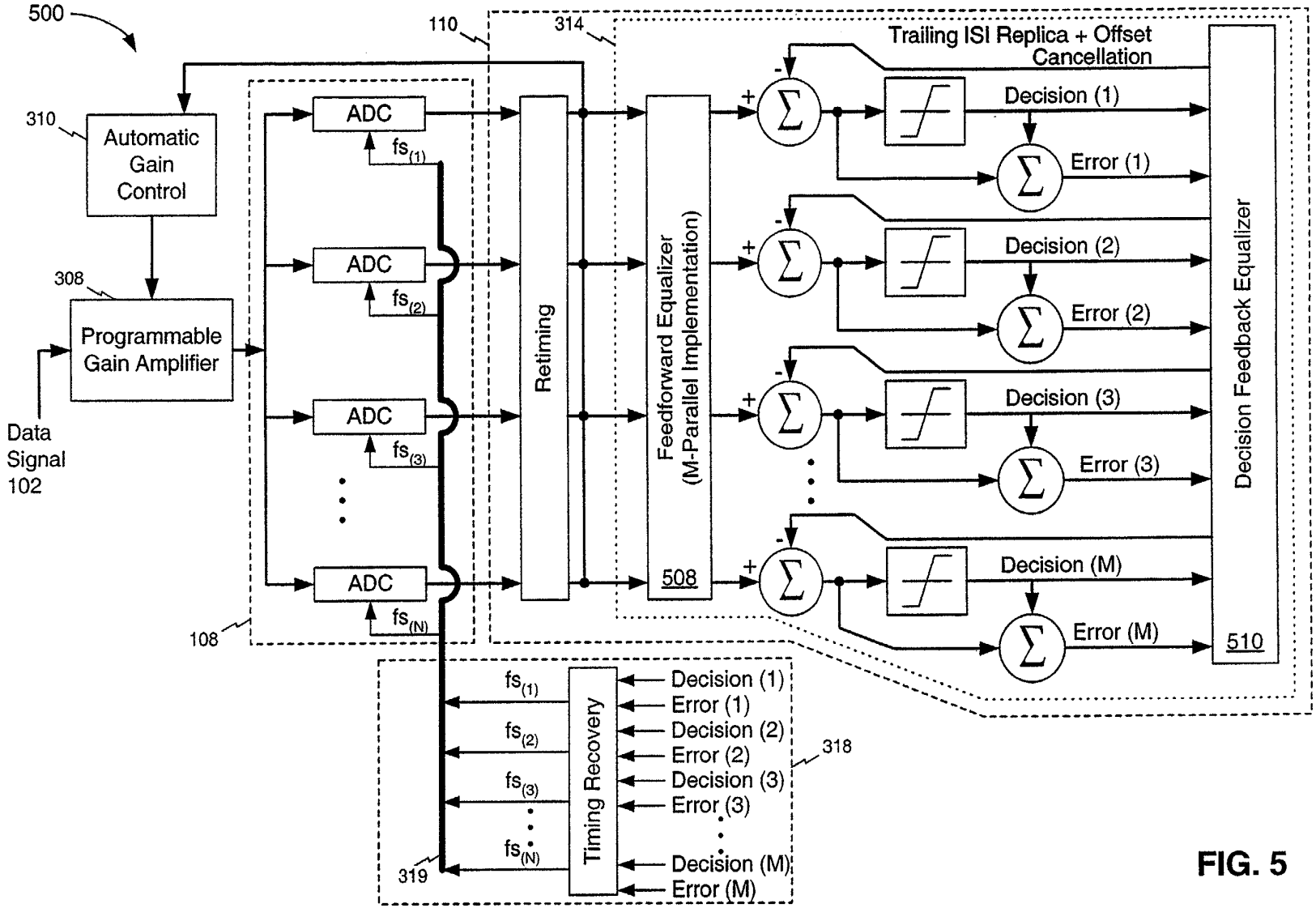

500
110
314
Trailing ISI Replica + Offset Cancellation
310
Automatic Gain Control
308
Programmable Gain Amplifier
Data Signal 102
ADC
ADC
ADC
ADC
fs(1)
fs(2)
fs(3)
fs(N)
Retiming
Feedforward Equalizer (M-Parallel Implementation)
508
Decision (1)
Error (1)
Decision (2)
Error (2)
Decision (3)
Error (3)
Decision (M)
Error (M)
Decision Feedback Equalizer
510
108
318
319
Timing Recovery

FIG. 5

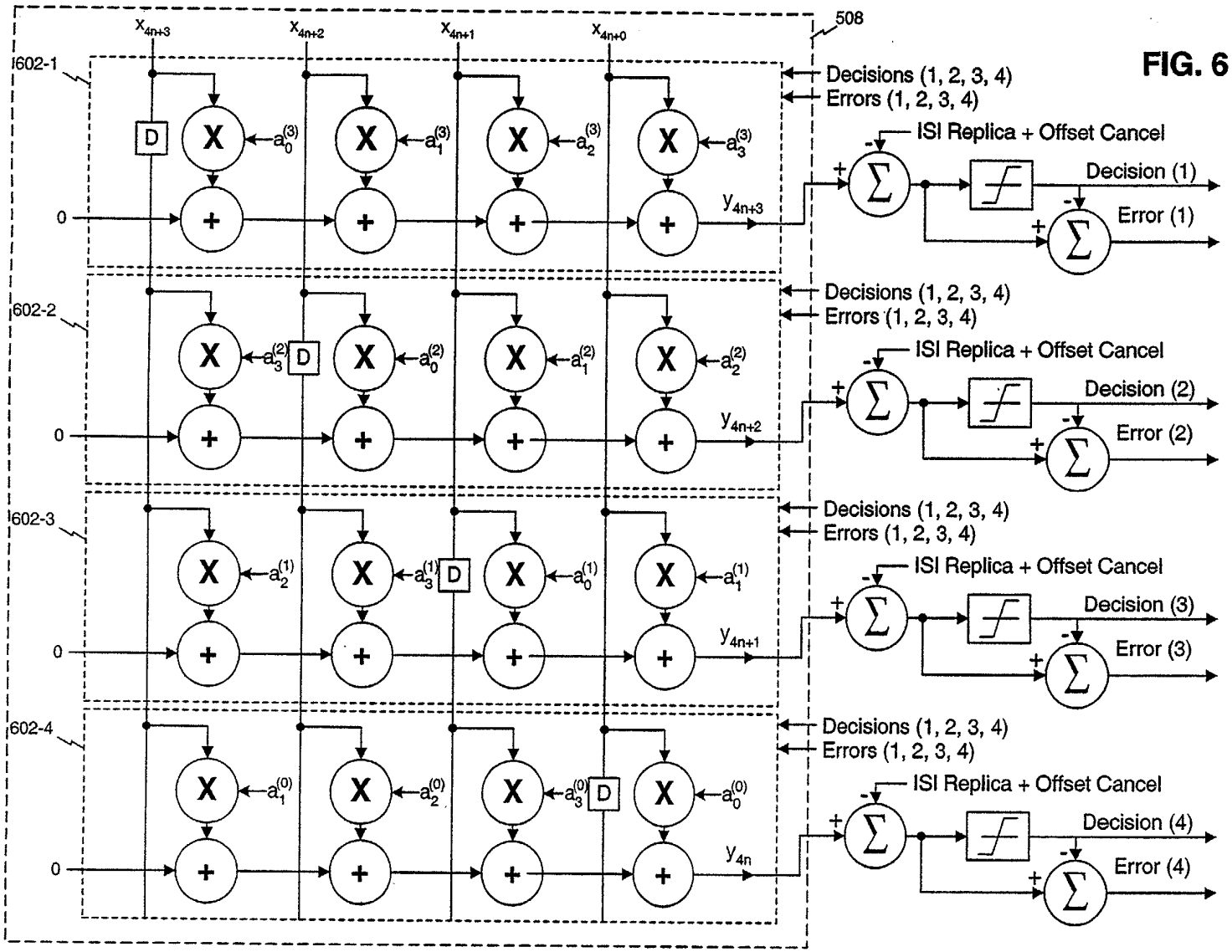


FIG. 6

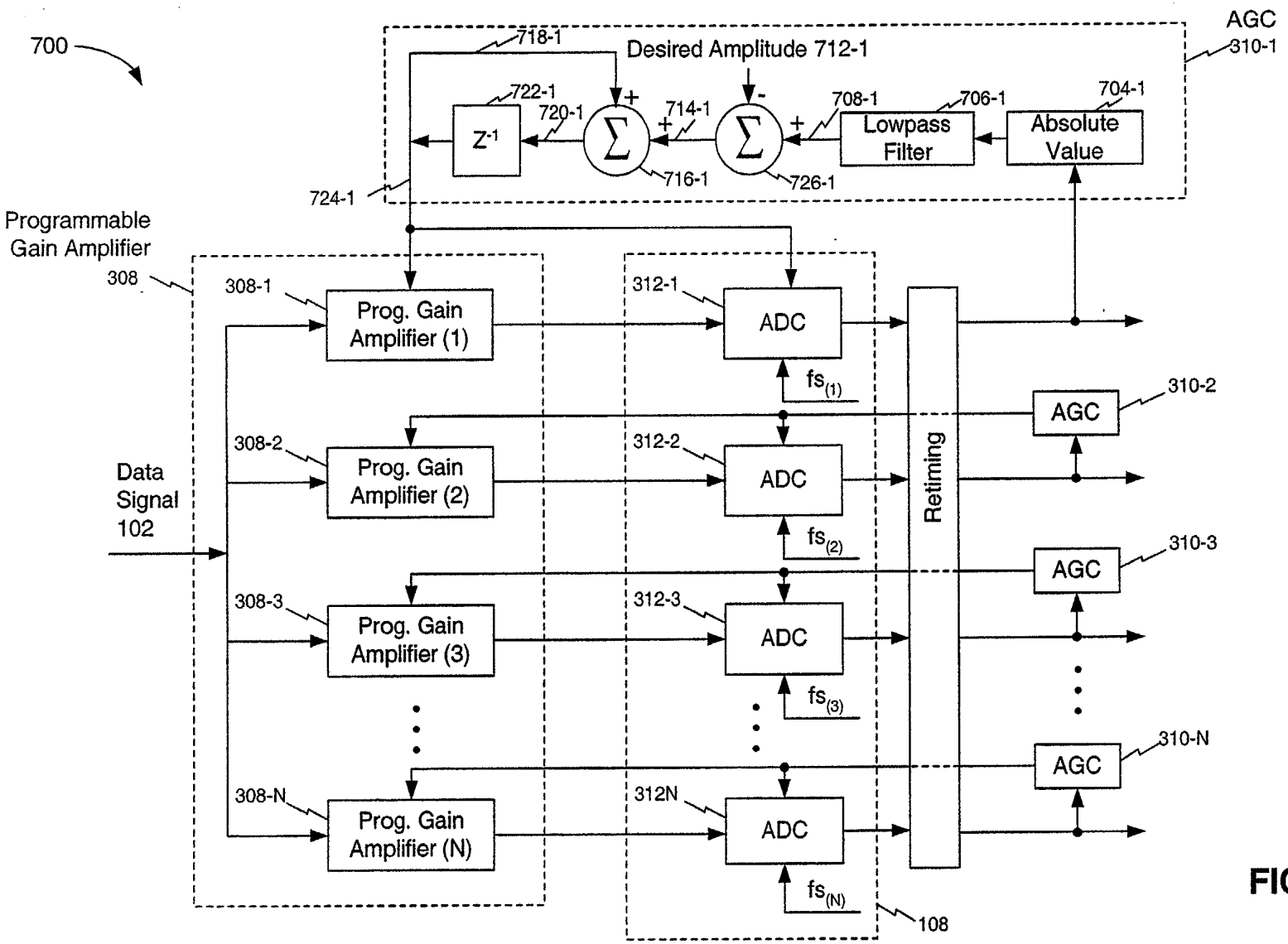

700
AGC
310-1
718-1
Desired Amplitude 712-1
722-1
720-1
714-1
708-1
706-1
704-1
Z-1
Lowpass Filter
Absolute Value
716-1
726-1
724-1
Programmable Gain Amplifier
308
308-1
Prog. Gain Amplifier (1)
312-1
ADC
fs(1)
310-2
AGC
308-2
Prog. Gain Amplifier (2)
312-2
ADC
fs(2)
Data Signal 102
Retiming
310-3
AGC
308-3
Prog. Gain Amplifier (3)
312-3
ADC
fs(3)
310-N
AGC
308-N
Prog. Gain Amplifier (N)
312N
ADC
fs(N)
108

FIG. 7

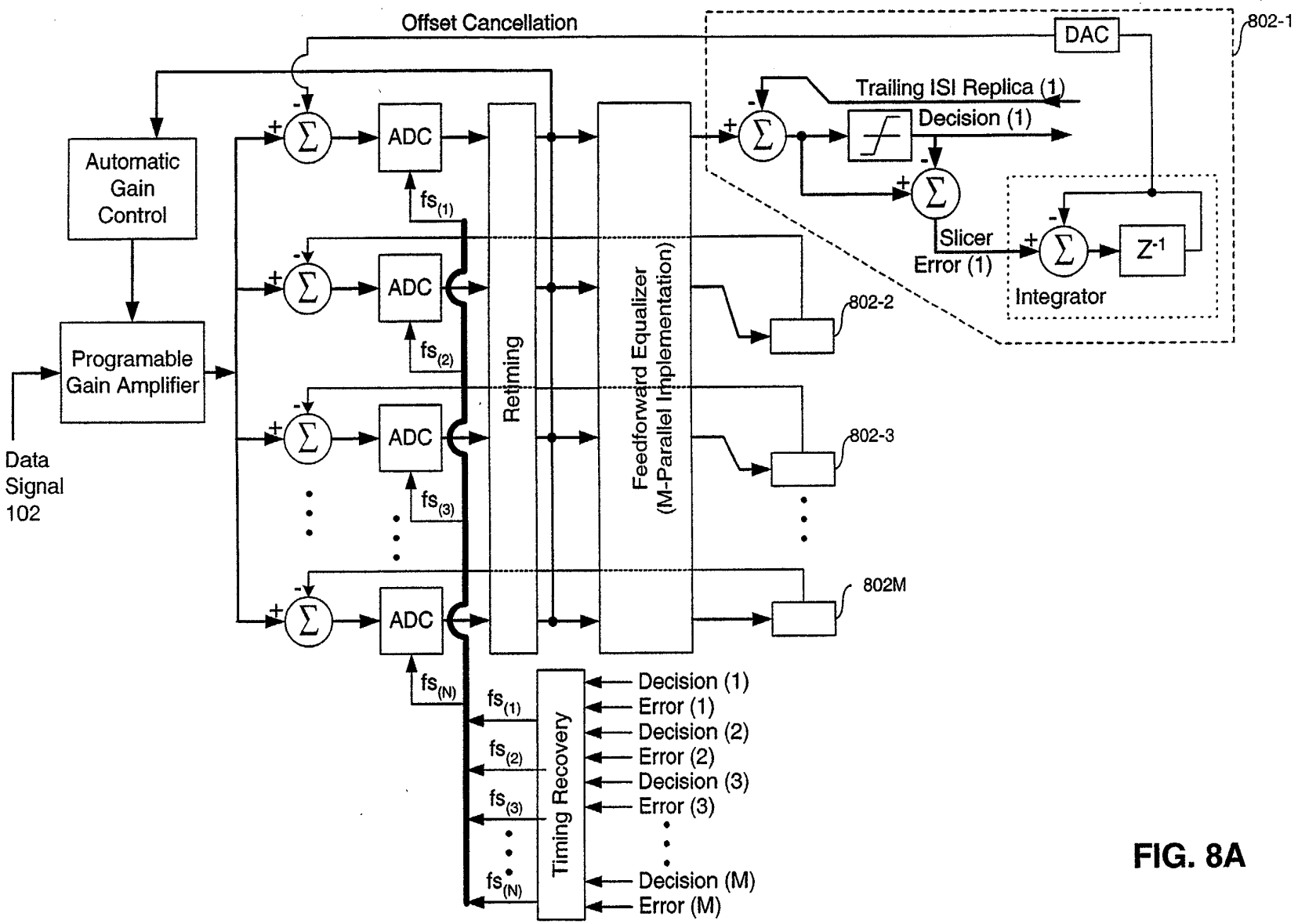

Offset Cancellation
802-1
DAC
Trailing ISI Replica (1)
Decision (1)
Slicer
Error (1)
Integrator
Z^{-1}
Automatic Gain Control
Programable Gain Amplifier
Data Signal 102
ADC
$fs_{(1)}$
$fs_{(2)}$
$fs_{(3)}$
$fs_{(N)}$
Retiming
Feedforward Equalizer (M-Parallel Implementation)
802-2
802-3
802M
Timing Recovery
Decision (1)
Error (1)
Decision (2)
Error (2)
Decision (3)
Error (3)
Decision (M)
Error (M)

FIG. 8A

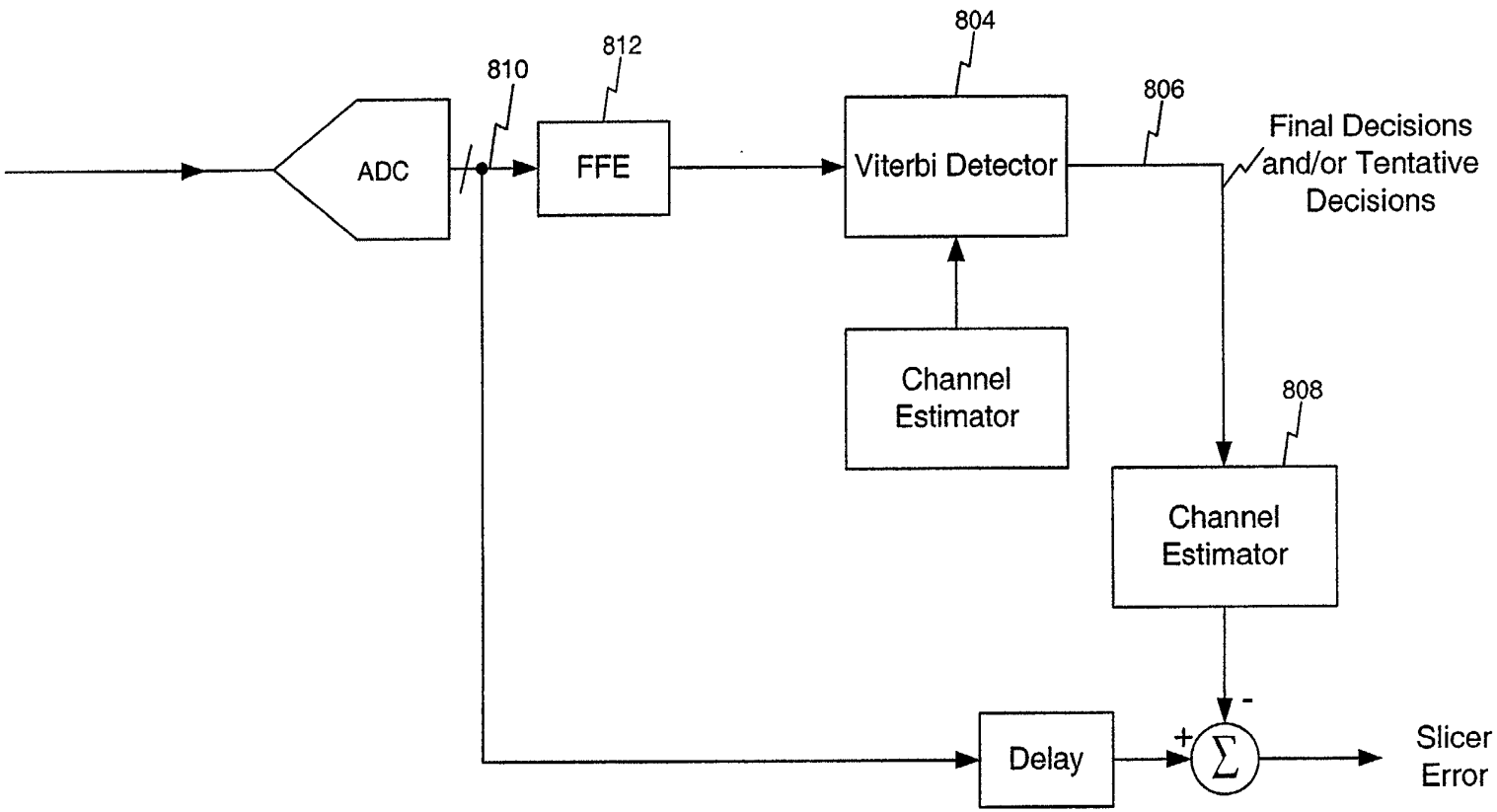

804
812
810
806
ADC
FFE
Viterbi Detector
Final Decisions
and/or Tentative
Decisions
Channel
Estimator
808
Channel
Estimator
-
+
Delay
Σ
Slicer
Error

FIG. 8B

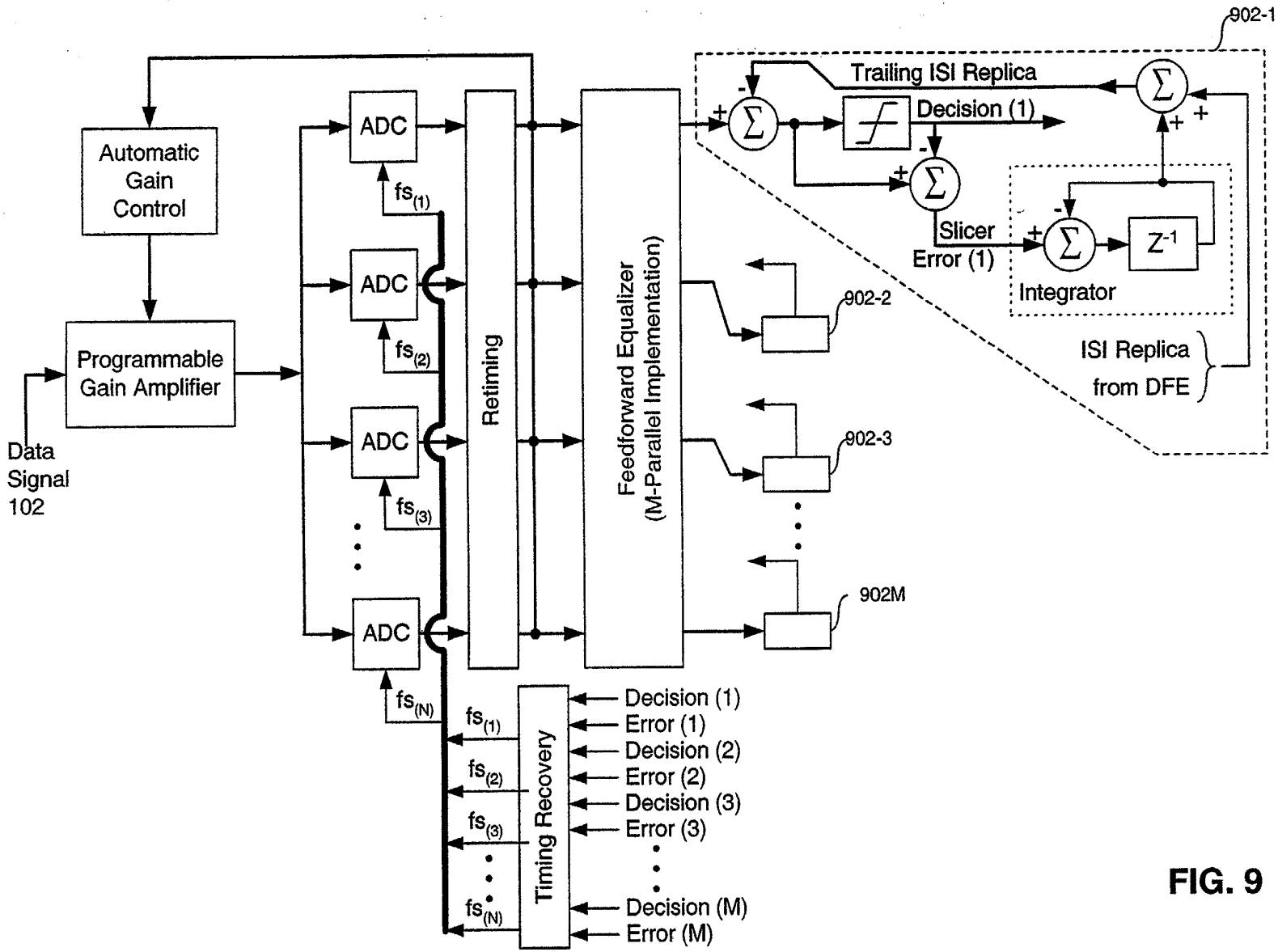


FIG. 9

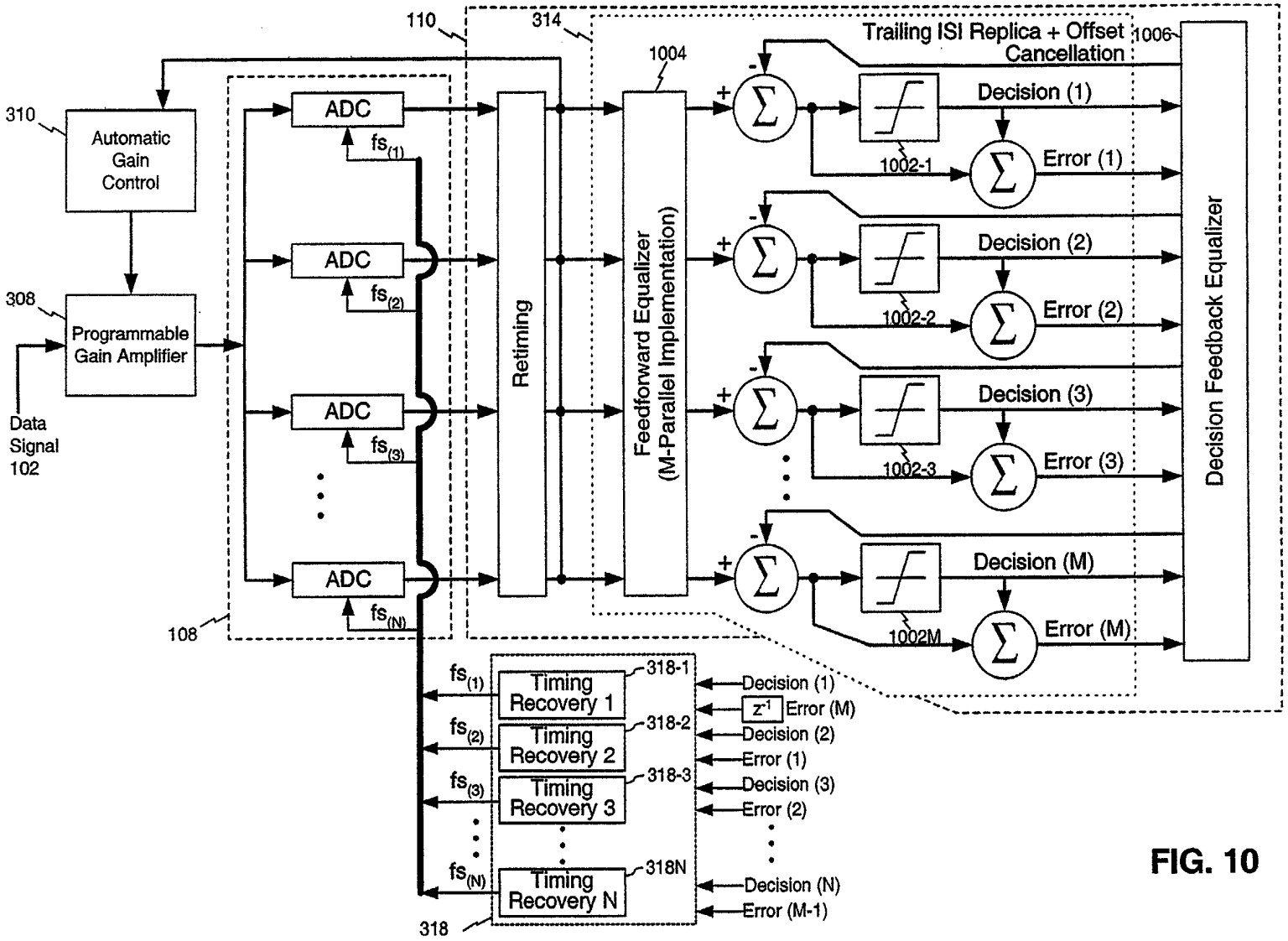

110
314
1004
Trailing ISI Replica + Offset Cancellation
1006
310
Automatic Gain Control
308
Programmable Gain Amplifier
Data Signal 102
ADC
ADC
ADC
ADC
fs(1)
fs(2)
fs(3)
fs(N)
108
Retiming
Feedforward Equalizer (M-Parallel Implementation)
Decision (1)
Error (1)
Decision (2)
Error (2)
Decision (3)
Error (3)
Decision (M)
Error (M)
1002-1
1002-2
1002-3
1002M
Decision Feedback Equalizer
Timing Recovery 1
Timing Recovery 2
Timing Recovery 3
Timing Recovery N
318-1
318-2
318-3
318N
318
z-1
Error (M)
Decision (2)
Error (1)
Decision (3)
Error (2)
Decision (N)
Error (M-1)

FIG. 10

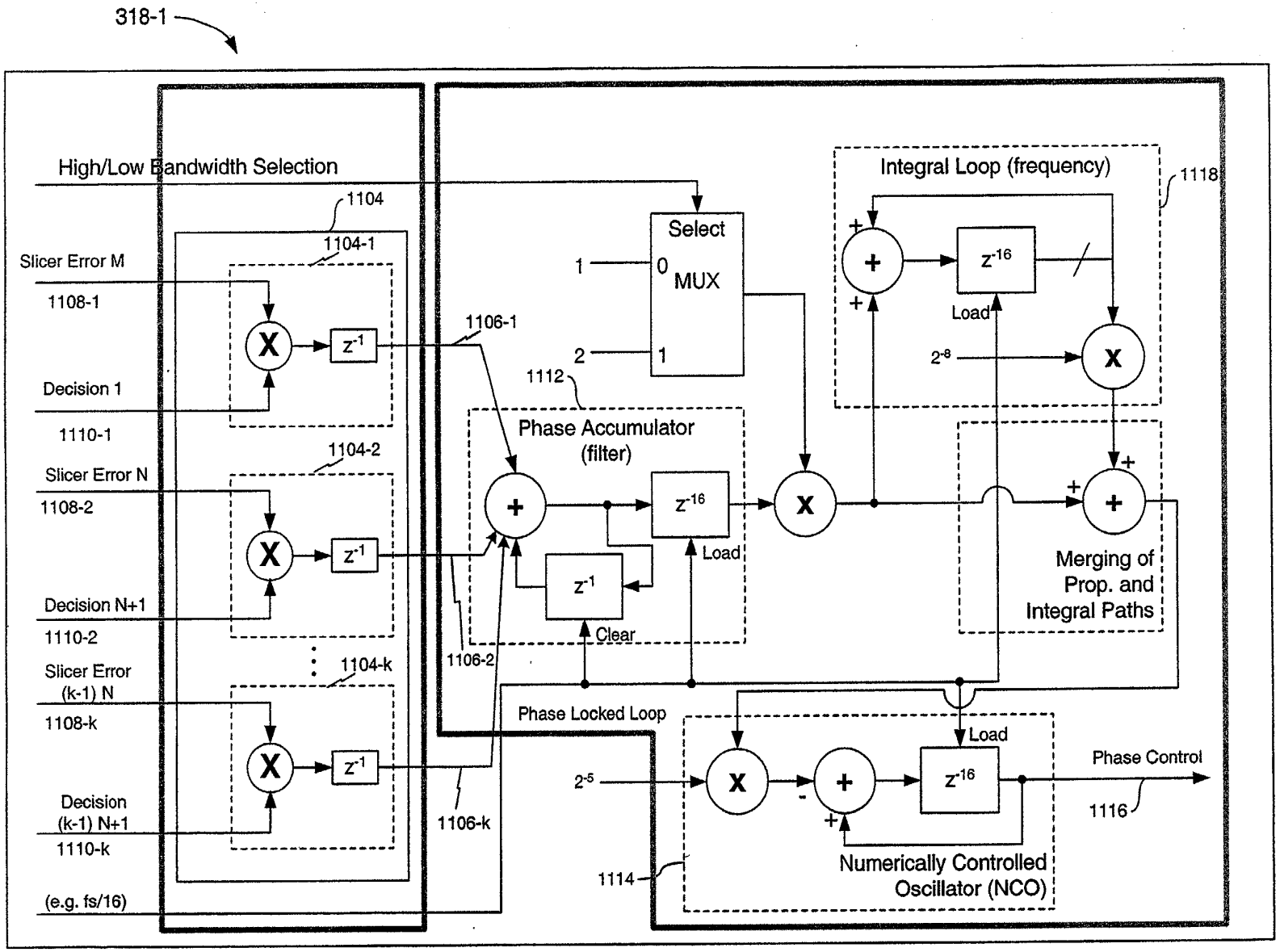


FIG. 11 Timing Recovery

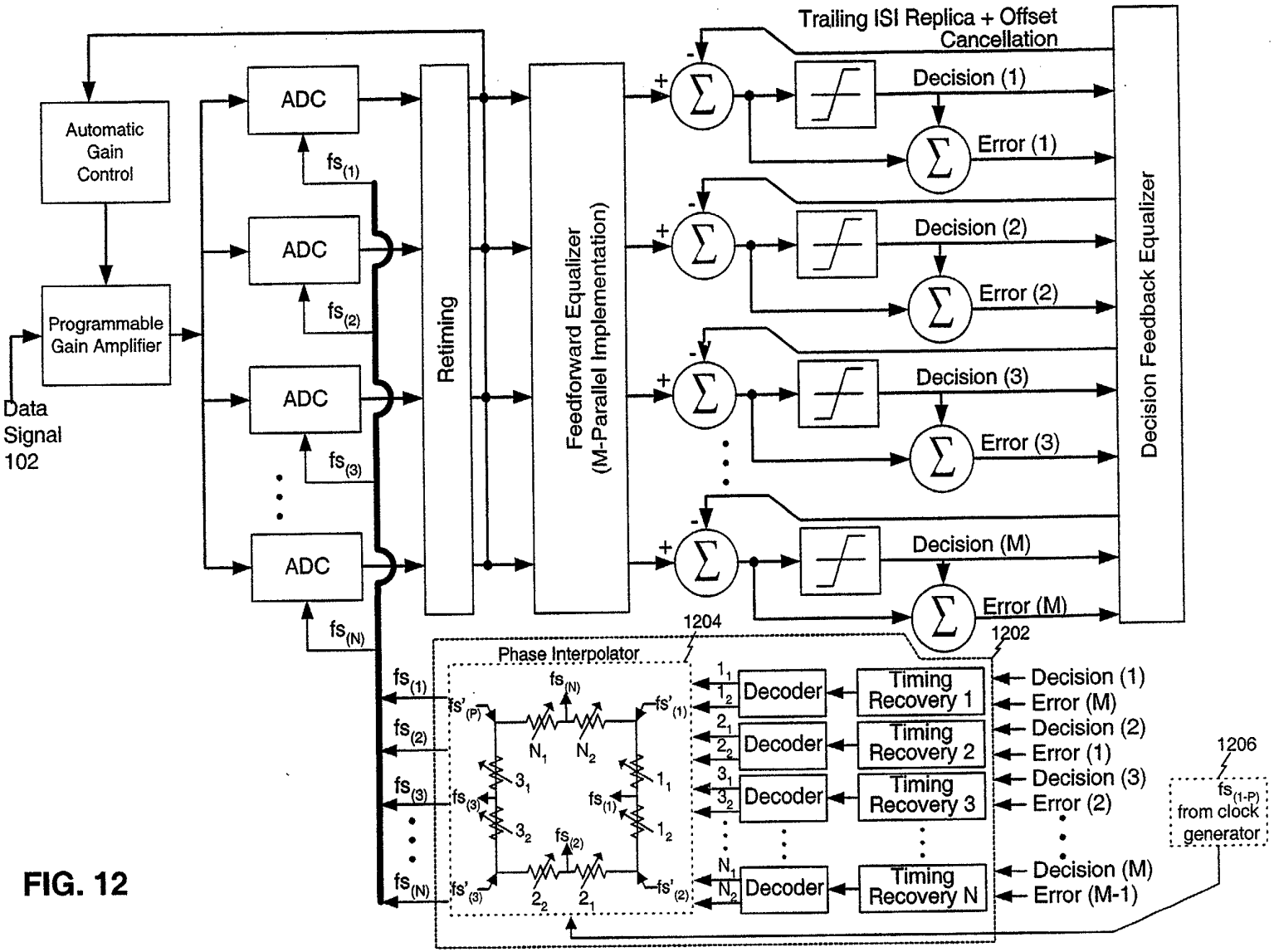
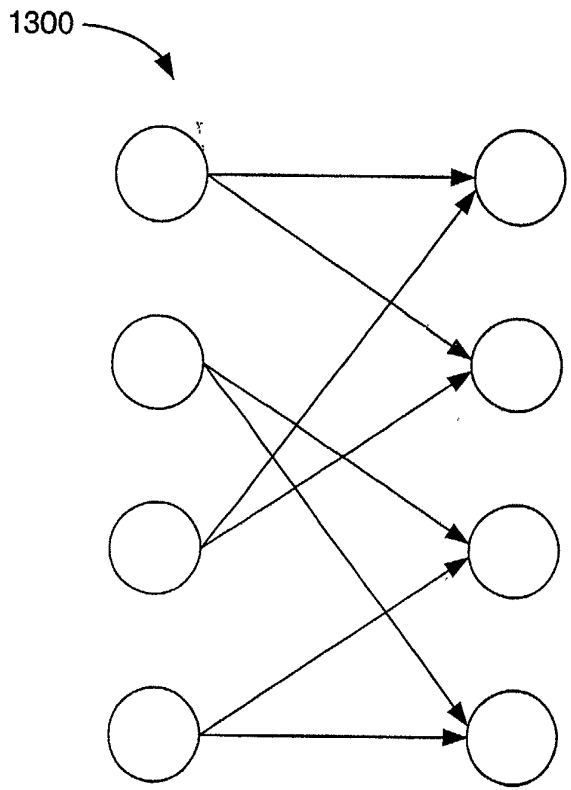
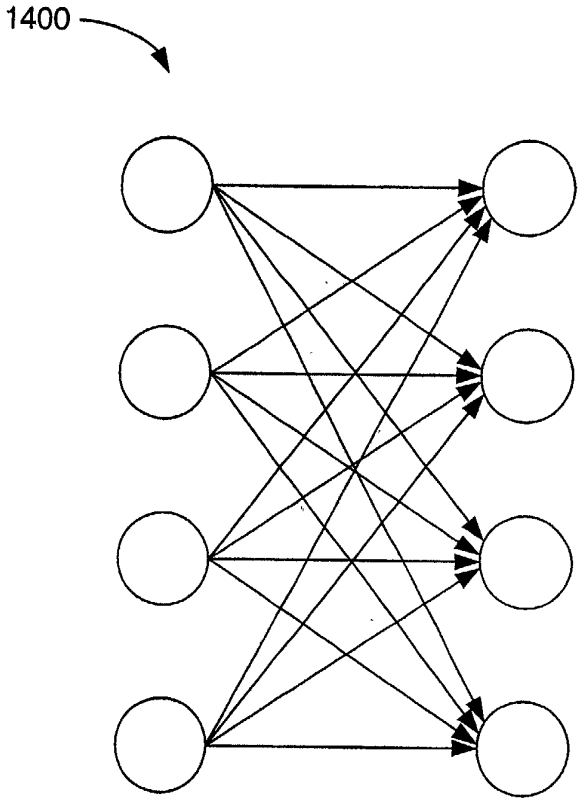


FIG. 12



4-state 1-step trellis (runs at a clock rate equal to the symbol rate)

FIG. 13



4-state M-step trellis (runs at a clock rate equal to 1/M of the symbol rate)

FIG. 14

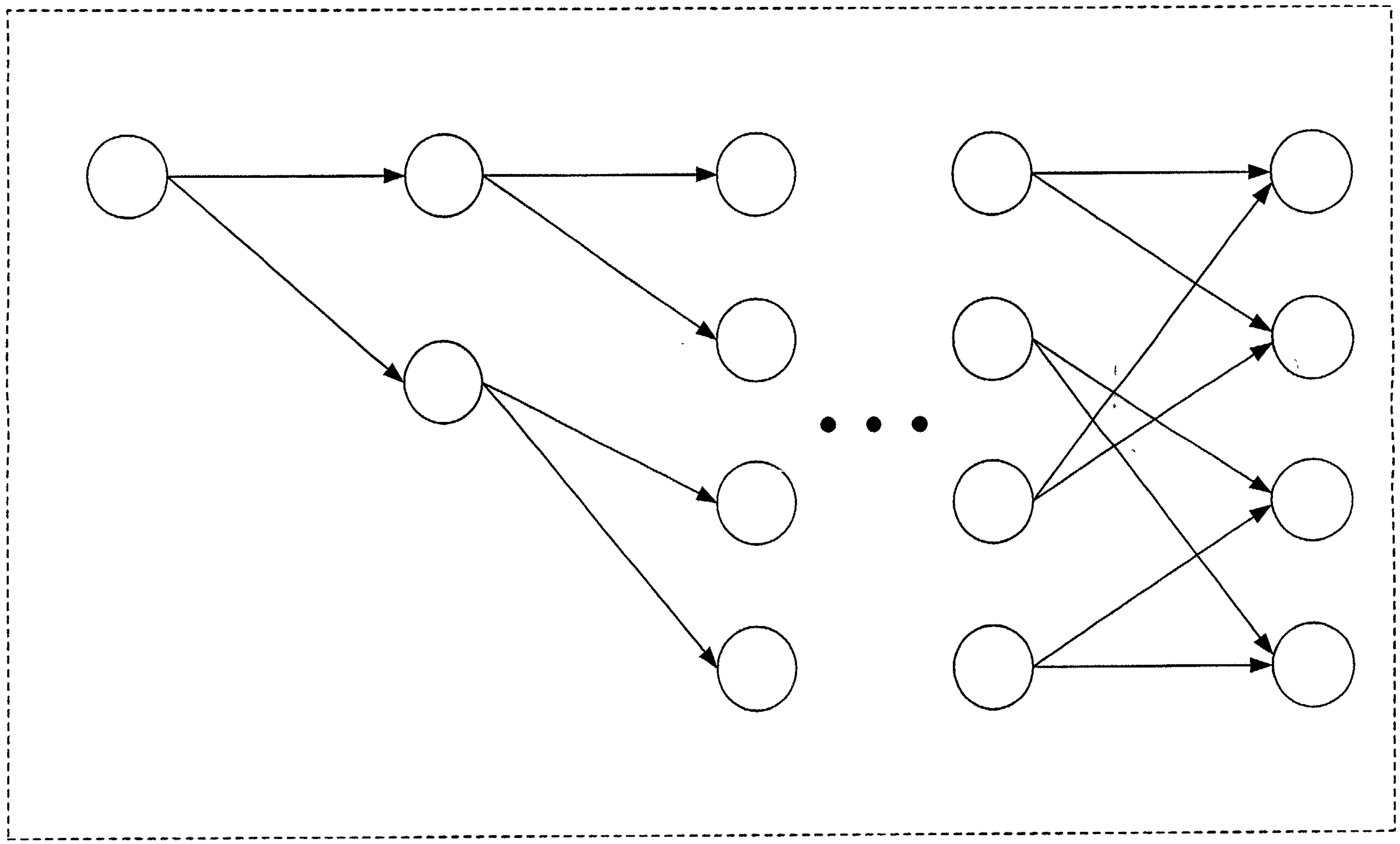


FIG. 15A

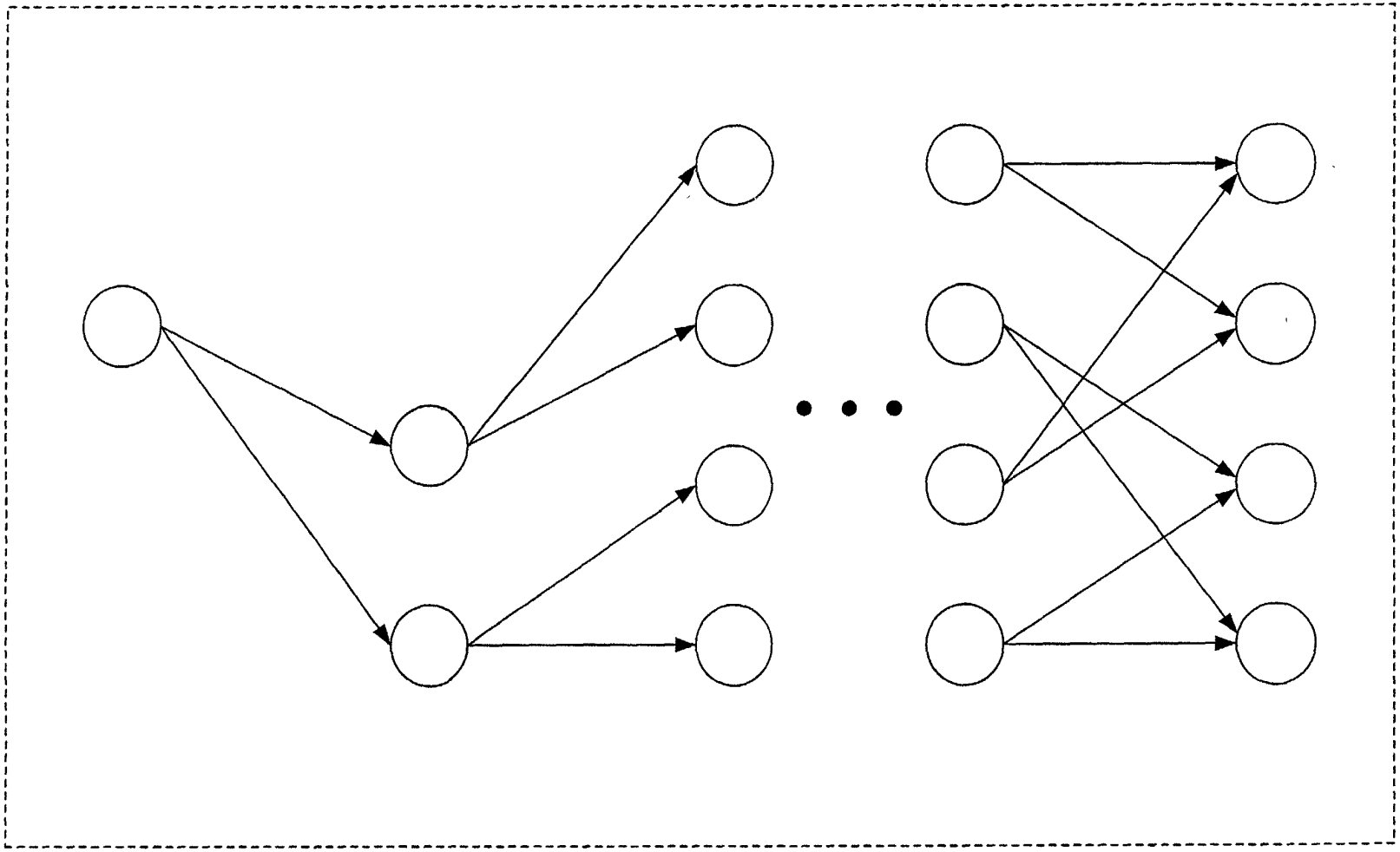


FIG. 15B

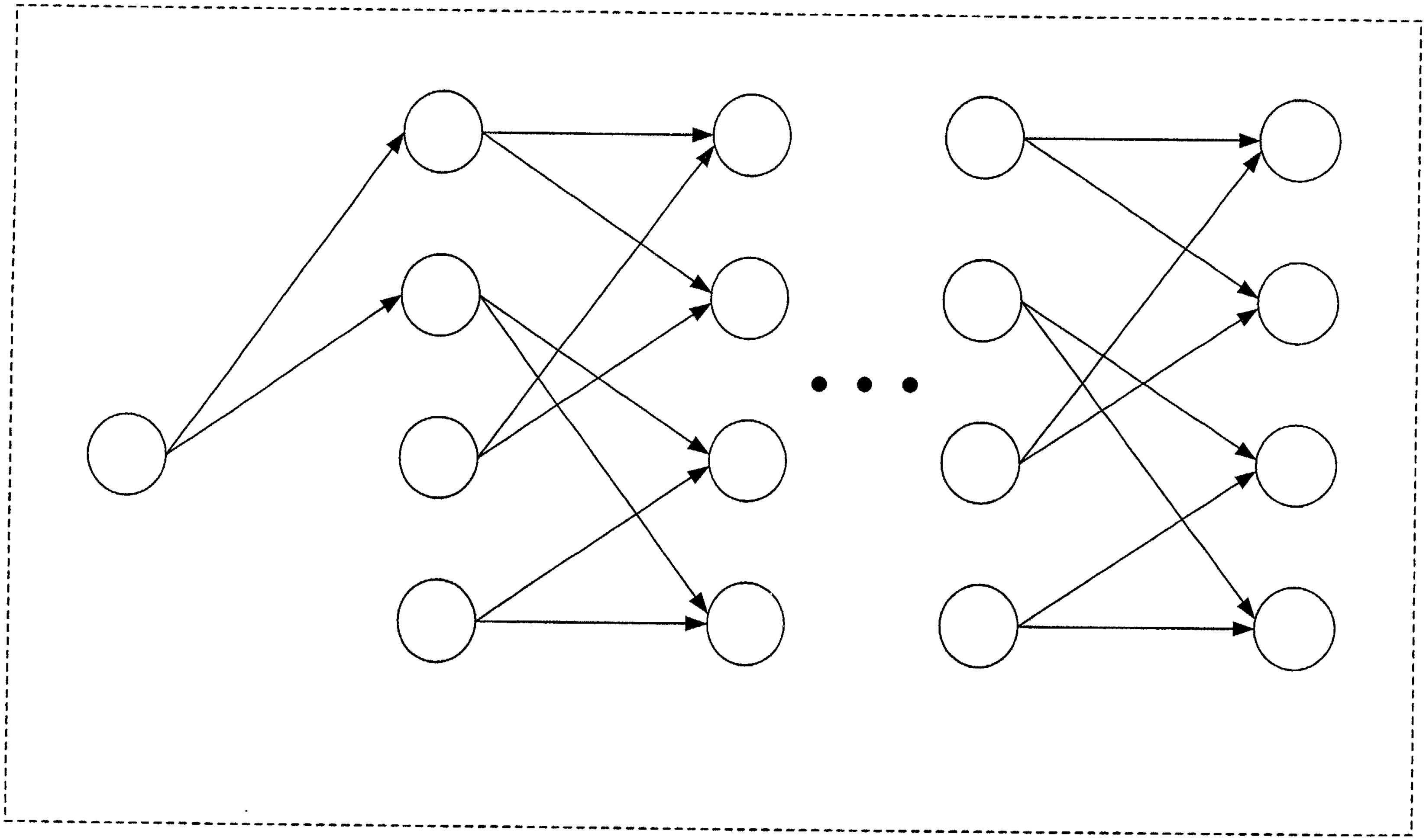


FIG. 15C

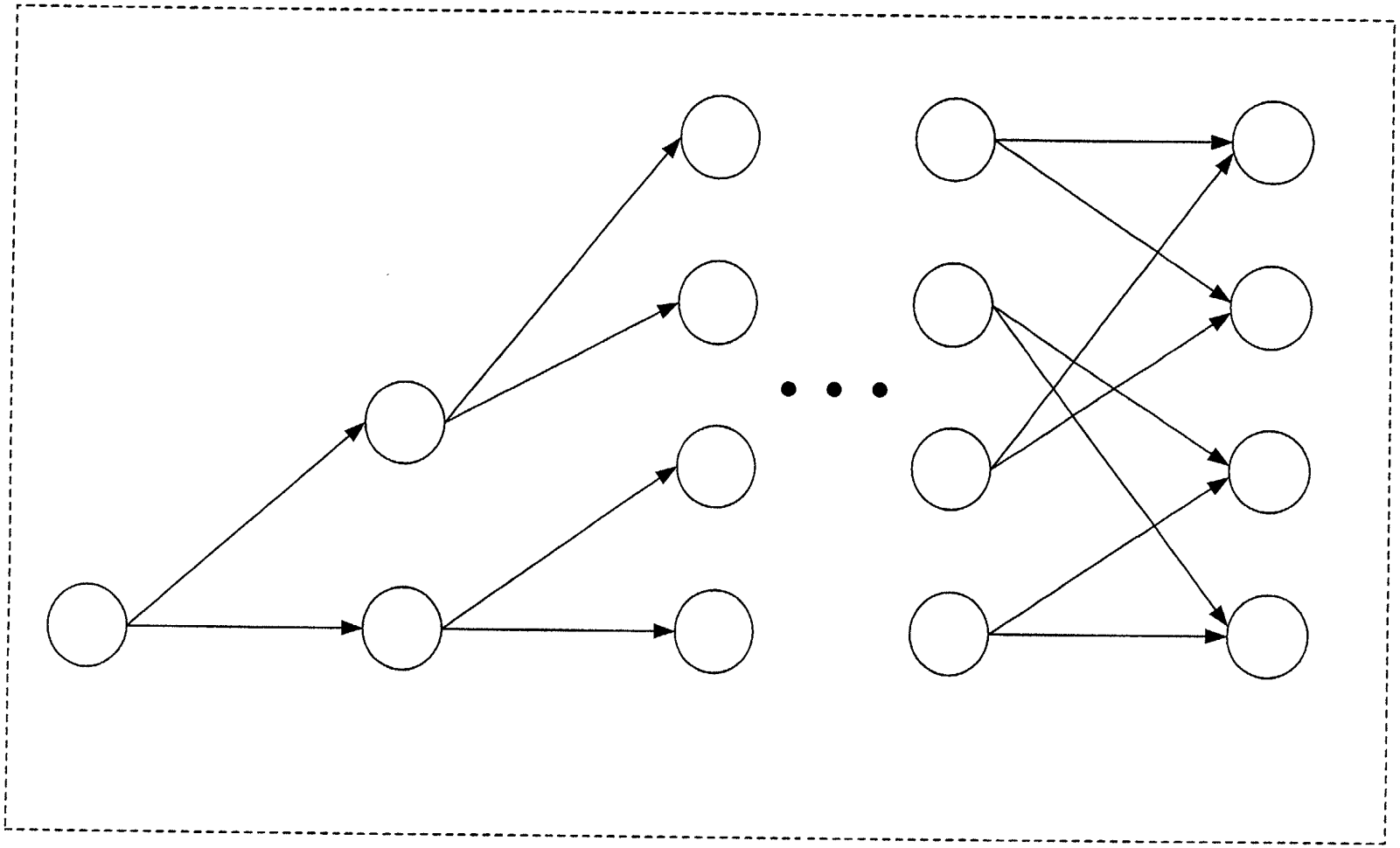
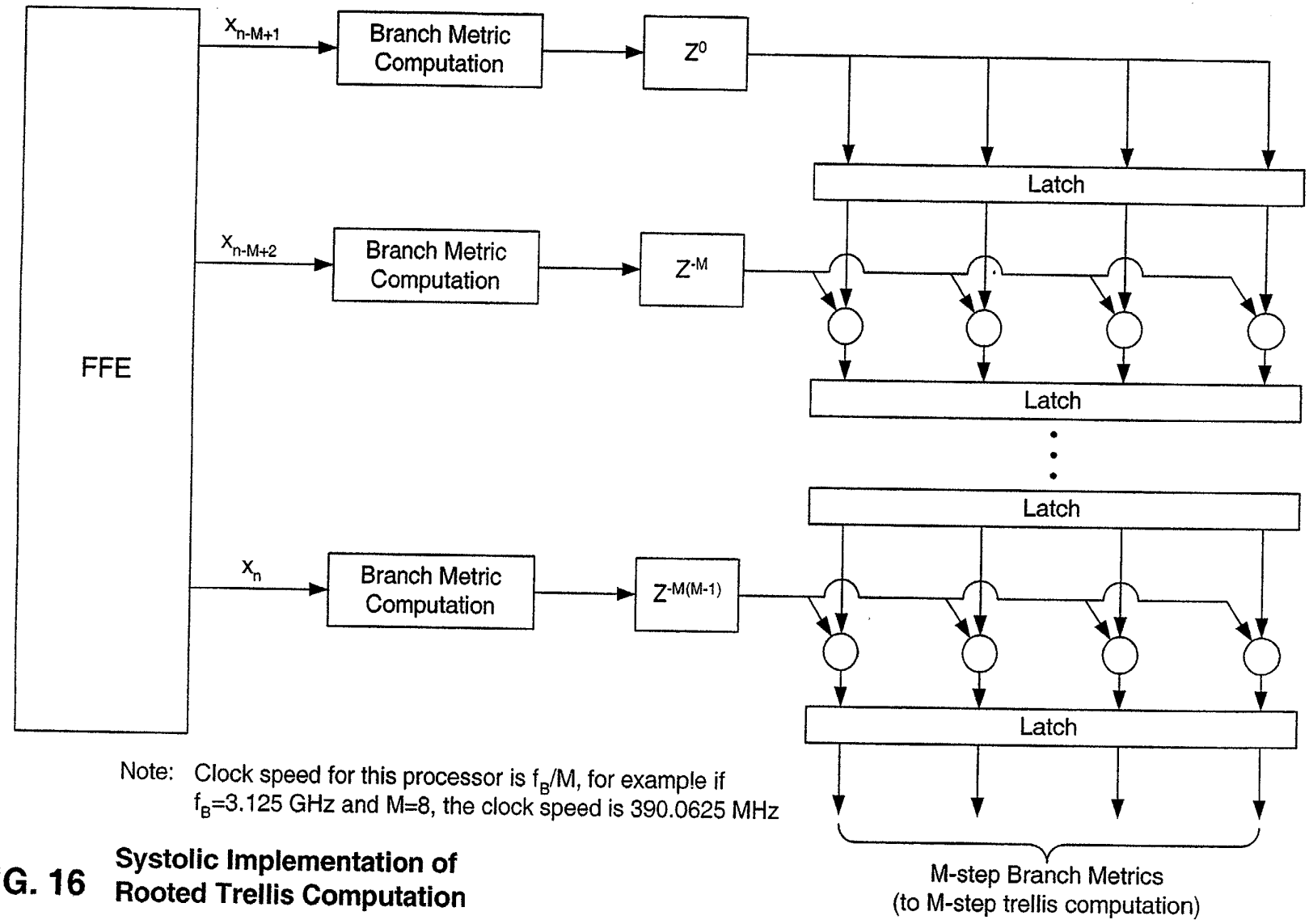


FIG. 15D



Note: Clock speed for this processor is f_B/M, for example if f_B=3.125 GHz and M=8, the clock speed is 390.0625 MHz

FIG. 16 **Systolic Implementation of Rooted Trellis Computation**

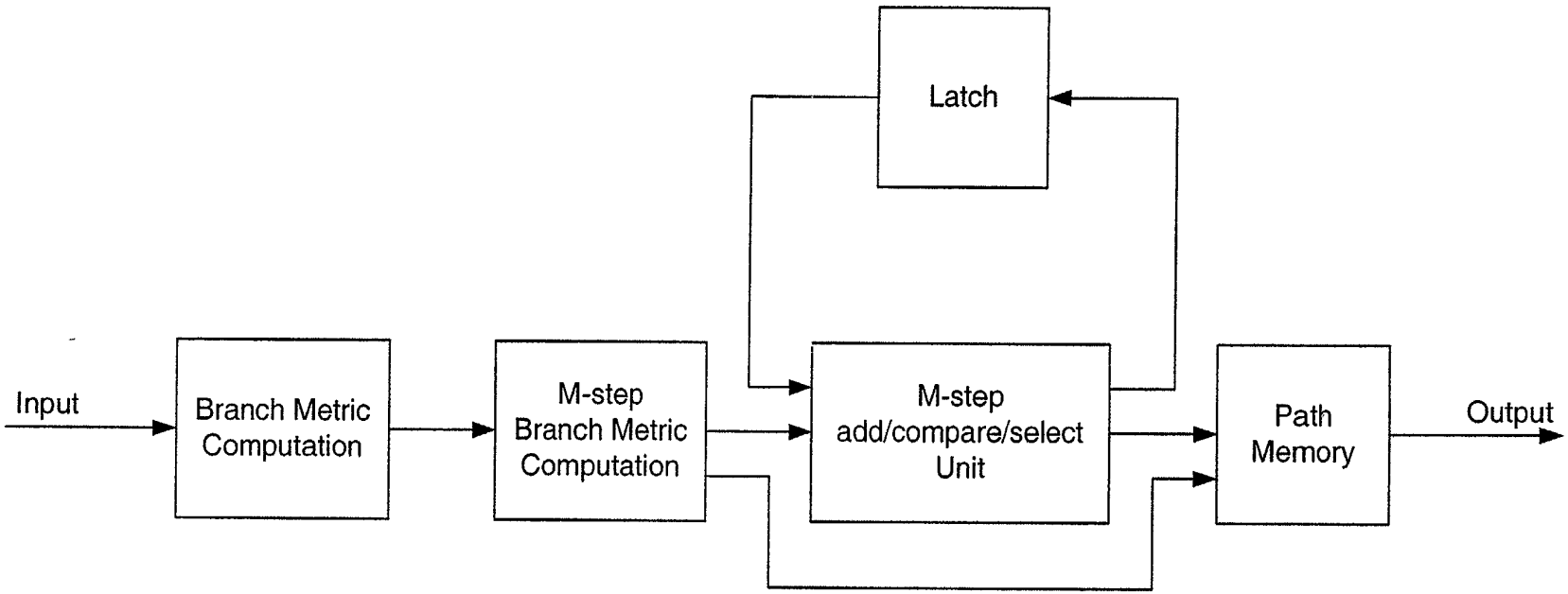


FIG. 17 **Overall Block Diagram of Parallel Viterbi Processor**

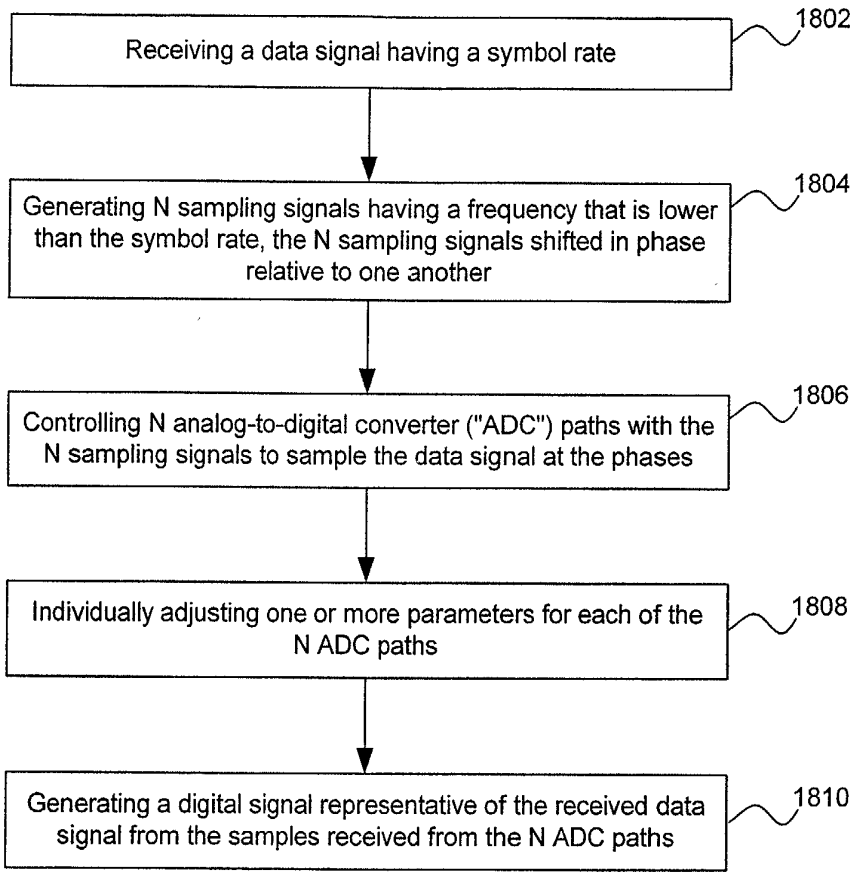

Receiving a data signal having a symbol rate
1802
Generating N sampling signals having a frequency that is lower than the symbol rate, the N sampling signals shifted in phase relative to one another
1804
Controlling N analog-to-digital converter ("ADC") paths with the N sampling signals to sample the data signal at the phases
1806
Individually adjusting one or more parameters for each of the N ADC paths
1808
Generating a digital signal representative of the received data signal from the samples received from the N ADC paths
1810

FIG. 18